In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): A liquid crystal display device with a capacitance-compensated structure, comprising:

a gate line;

a gate electrically connected to the gate line;

a compensation structure extending from at least one of the gate and the gate line;

a drain having a first side and a second side, wherein the first side of the drain overlaps a portion of the gate and the second side of the drain overlaps a portion of the compensation structure ; and

a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure.

2-3. (cancelled).

4. (previously presented): The device of claim 1, wherein the compensation structure comprises two portions, in which one extends from the gate line and the other extends from the gate.

5. (currently amended): A liquid crystal display device with a capacitance-compensated structure, having a gate line and a data line to turn a thin film transistor on or off, comprising:

a gate electrically connected to the gate line;

a drain having a first side and a second side, wherein a first parasitic capacitor is formed between the first side of the drain and the gate and a second parasitic capacitor is formed between the second side of the drain and the gate, wherein the second parasitic capacitor comprises the second side of the drain and a compensation structure extending from at least one of the gate and the gate line; and

a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the capacitance-compensation structure and substantially spaced apart from at least one of the gate and the capacitance-compensation structure.

6. (previously presented): The device of claim 5, wherein a capacitor dielectric layer of the first parasitic capacitor comprises two portions, wherein one portion is a stacked structure comprising a gate insulating layer, a semiconductor layer, and a

channel protection layer, and the other portion is a stacked structure comprising the gate insulating layer and the semiconductor layer, a capacitor dielectric layer of the second parasitic capacitor is a stacked structure comprising the gate insulating layer and the semiconductor layer.

7-9. (cancelled).

10. (previously presented): The device of claim 5, wherein the compensation structure comprises two portions, wherein one portion extends from the gate line and the other portion extends from the gate.

11. (currently amended): A liquid crystal display device with a capacitance-compensated structure, comprising:

a first process layer comprising a gate line, a gate, and a compensation structure, wherein the gate is electrically connected to the gate line and the compensation structure connects to the gate;

a second process layer comprising a data line, a source, and a drain, wherein the source and the drain are formed corresponding to both sides of the gate, respectively, the source is electrically connected to the data line, the data line is substantially perpendicular to the gate line, the drain has a first side overlapping a portion of the gate and a second side overlapping a portion of the compensation structure; and

a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure;

wherein there is an acceptable alignment shift range between the first process layer and the second process layer, the sum of the capacitance of a first parasitic capacitor between the first side of the drain and the gate and a second parasitic capacitor between the second side of the drain and the compensation structure maintain a substantially constant value within the acceptable alignment shift range.

12. (previously presented): The device of claim 11, wherein the compensation structure extends from the gate line.

13. (previously presented): The device of claim 11, wherein the compensation structure extends from the gate.

14. (previously presented): The device of claim 11, wherein the compensation structure comprises two portions, wherein one portion extends from the gate line and the other portion extends from the gate.

15. (Canceled):

16. (previously presented): The device of claim 1, wherein the first side is substantially opposite to the second side.

17. (canceled): The device of claim 5, wherein the pixel electrode is substantially located between the gate and the capacitance-compensation structure and substantially spaced apart from at least one of the gate and the capacitance-compensation structure.

18. (previously presented): The device of claim 5, wherein the first side is substantially opposite to the second side.

19. (canceled): The device of claim 11, wherein the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure.

20. (previously presented): The device of claim 11, wherein the first side is substantially opposite to the second side.